UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,156	10/25/2001	James D. Beasom	125.020US01	7041

34206 7590 08/25/2004

FOGG AND ASSOCIATES, LLC
P.O. BOX 581339
MINNEAPOLIS, MN 55458-1339

EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,156	BEASOM, JAMES D.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Cancellations

1. Applicant's cancellation of Claims 13 and 18 in Letter of June 1, 2004 is acknowledged.

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 12 are rejected under 35 U.S.C. 103(a) as being anticipated by Tu et al. (US 6,486,033 B1) in view of Wu (US 5,679,601).

4. Regarding Claim 1,Tu et al. disclose a method wherein a nitride sealing layer (first layer) (Figure 8) (24) (Col. 4, lines 20 – 25) is formed overlying an oxide (Col. 3, lines 36 – 38) layer in a contact opening of an integrated circuit, the method comprising:

forming a second layer of nitride (Col. 4, lines 27 – 30) (28) (Figure 8) overlaying the first nitride layer (24) and without any intervening layers between the first and second nitride layers to form a sealing layer, and further overlaying an exposed portion of the substrate and sidewalls of the opening (Figure 8).

Tu et al. do not disclose using RIE etch without a mask to remove a portion of the second nitride layer adjacent the surface of the substrate in the contact opening without removing portions of the second nitride layer covering the sidewalls of the contact opening. Wu discloses (Col. 4, lines 3 – 5) that RIE (without a mask) is used to remove portions of the nitride In the adjacent areas without removing portions of the nitride covering sidewalls. It would have then been obvious to one of ordinary skill in the art at the time of the invention to combine the RIE procedures of Wu with Tu et al. to obtain an efficient means for obtaining a sealing nitride layer residing on sidewalls of the gate layers.

5. Regarding Claim 2, Tu et al. do not explicitly disclose that the nitride layer is deposited by LPCVD. Wu discloses formation of the second nitride layer by LPCVD (Col. 3, line 66 through Col. 4, line 3). It would have been obvious to combine Wu and Tu et al. to obtain uniform and higher deposition rate films.

6. Regarding Claim 3, Tu et al. do not disclose that the second nitride layer is formed by plasma enhanced chemical vapor deposition (PECVD). However, Wu discloses that PECVD (Col. 3, lines 66 – 67, Col.4, lines 1 – 5) is used to form the second sealing nitride layer (22) (Figure 6). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wu and Tu et al. to obtain a PECVD nitride layer of controlled density to reduce indiffusion of contaminants to the active device area.

7. Regarding Claim 4, Tu et al. disclose (Figure 8) that a portion of the first nitride layer (24) remains overlying the oxide (Col. 3, lines 36 – 38) after RIE (etching) is applied.

8. Regarding Claims 5 and 6, neither Tu et al. nor Wu disclose the times required to perform the task of removing the nitride overlaying the surface of the substrate without removing portions of the nitride layer overlaying portions of the sidewalls during RIE. It would have been obvious to one of ordinary skill in the art at the time of the invention to adjust the times of etch to avoid removing all of the layer from sidewalls. Since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimal or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

9. Regarding Claim 7, as discussed previously, Tu et al. disclose a method for forming an integrated circuit, the method comprising:

forming a layer of oxide over a surface of a substrate (Col. 3, lines 36 – 38),

forming a first layer of nitride (24) (Figure 8) (Col. 4, lines 20 – 25) overlaying the oxide,

forming a contact opening through the first layer of nitride and oxide layer (Col. 4, lines 22 - 25) to "expose" a portion of the substrate, and

forming a second layer of nitride (28) overlaying the first layer of nitride (24), the second layer of nitride also overlaying the "exposed" portion of the surface of the substrate in the contact opening and sidewalls of the contact opening.

Tu et al. do not disclose using RIE etch without a mask to remove a portion of the second nitride layer adjacent the surface of the substrate in the contact opening without removing portions of the second nitride layer covering the sidewalls of the contact opening and without removing portions of the first nitride layer overlaying the oxide layer. Tu et al. do disclose (Col. 4, lines 35 – 38) that "etching" is done, after second nitride deposition, to form contact openings in the memory section (7) (right side, Figure 8) Wu discloses (Col. 4, lines 3 – 5) that RIE (without a mask) is used to remove portions of the nitride in the adjacent areas without removing portions of the nitride covering sidewalls (Figure 7) and that the oxide layer (12) is sealed by the first and second nitride layers (14/22) (Figures 4 - 6). It would have then been obvious to one of ordinary skill in the art at the time of the invention to combine the RIE procedures of Wu with Tu et al. to obtain a sealing nitride layer residing on sidewalls of the gate layers.

Neither Tu et al. nor Wu disclose the times required to perform the task of removing the nitride overlaying the surface of the substrate without removing portions of the nitride layer overlaying portions of the sidewalls during RIE. It would have been obvious to one of ordinary skill in the art at the time of the invention to adjust the times of etch to avoid removing all of the layer from sidewalls. Since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimal or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

10. Regarding Claim 8, Tu et al. disclose (Col. 4, lines 23 – 25) that the contact openings through the nitride and oxide layers are done with a dry etch with one photoresist mask.

11. Regarding Claim 9, Tu et al. disclose (Col. 3, lines 36 –38) the formation of a thermally grown oxide layer.

12. Regarding Claim 10, Tu et al. disclose that functional devices within the integrated circuit are formed with a thermal oxide as the interfacial layer, but do not disclose that the oxide layer is "deposited." The formation of oxide layers by deposition is extremely well known in the art and commercial equipment readily available (for example, Applied Materials, Novellus, Lam Research and others). Therefore, it would have been obvious to one of routine skill in the art at the time of the invention to utilize deposited films of oxide for efficiency in the production process.

13. Regarding Claim 11, Tu et al. do not disclose that the first and second nitride layers are formed by LPCVD. Wu discloses that the first nitride layer (14) is formed by LPCVD (Col. 3, lines 23 – 25) and that the second nitride layer (22) is formed by LPCVD (Col. 3, line 66 through Col. 4, line 3). It would have then been obvious to combine Wu with Tu et al. to obtain uniform nitride films.

14. Regarding Claim 12, Tu et al. disclose that functional devices within the integrated circuit are formed with LPCVD nitride layers. It would be obvious that PECVD could also be used to form the first and second layers of nitride, since both techniques produce a layer by CVD. In addition, commercial machines (Applied Materials,Novellus) are readily available in the art for plasma enhanced deposition. Therefore, it would have

been obvious to one of ordinary skill in the art at the time of the invention to form both nitride layers by PECVD to obtain high deposition rate films.

15. Claims 14 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tu et al. in view of Wu, Leung et al. (US 6,573, 548 B2) and Wolf et al. ("Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Lattice Press, Sunset Beach, CA (1986), pp. 323 – 324).

18. Regarding Claim 14, Tu et al. disclose a method for forming semiconductor devices in an integrated circuit comprising:

forming a plurality of device regions in a substrate adjacent a surface of the substrate (Col. 2, lines 19 – 24),

forming an oxide layer over a surface of a substrate (Col. 3, lines 36 – 38),

patterning the oxide layer to expose pre-selected portions of the surface of the substrate (Figure 3),

forming a first layer of nitride overlaying the oxide and exposed portions of the surface of the substrate (Col. 4, lines 20 – 22),

implanting ions (Col. 4, lines 25 – 27) into the substrate to form source/drain device regions, wherein remaining portions of the oxide under the nitride selectively stop ions from entering the substrate to selectively define edges of the device regions (See Figure 8),

forming contact openings (Col. 4, lines 35 – 38) to expose a portion of the device regions containing first and second conductivity types (Figure 8, right side, substrate

and implanted area), and

forming a second layer of nitride (28) (Figure 8) over the first layer of nitride, the second layer of nitride also overlaying exposed portions of device regions in contact openings and sidewalls of each of the contact openings.

Tu et al. do not disclose using RIE etch to remove a portion of the second nitride layer adjacent the surface of the substrate in the contact opening without removing all portions of the second nitride layer covering the sidewalls of the contact opening and without removing portions of the first nitride layer overlaying the oxide layer, so that the oxide layer remains sealed by the first and second layers. Wu discloses (Col. 4, lines 3 – 5) that RIE is used to remove portions of the nitride in the adjacent areas without removing portions of the nitride covering sidewalls (Figure 7) and that the oxide layer (12) is sealed by the first and second nitride layers (14/22) (Figures 4 - 6). It would have then been obvious to one of ordinary skill in the art at the time of the invention to combine the RIE procedures of Wu with Tu et al. to obtain a sealing nitride layer residing on sidewalls of the gate layers.

Neither Tu et al. nor Wu disclose the times required to perform the task of removing the nitride overlaying the surface of the substrate without removing portions of the nitride layer overlaying portions of the sidewalls during RIE. It would have been obvious to one of ordinary skill in the art at the time of the invention to adjust the times of etch to avoid removing all of the layer from sidewalls. Since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimal or working ranges involves only routine

skill in the art. In re Aller, 105 USPQ 233.

Further, Tu et al. do not disclose a device region in a substrate of first conductivity type (n-type) and implantation of ions of second conductivity type (p-type) to form device regions. However, formation of devices using p-implants into n-type substrates or well regions is well known in the art. Leung et al. disclose (Figure 3N) that p type ions are implanted into an n-type device region (3011) to form a p-type device region (3036) for a memory cell application. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Leung et al. with Tu et al. to obtain a functional device within an integrated circuit.

Additionally, Tu et al. do not disclose that implants are done through the nitride layer. Surface layers are well known in the art (Wolf et al., p. 323, 1st para. under " Implanting Through Surface Layers") to provide a barrier for metals and other impurities introduced during processing. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wolf et al. with Tu et al. to provide a protective screen against metallic or other impurity contamination.

18. Regarding Claim 15, Tu et al. disclose (Col. 4, lines 23 – 25) that the contact openings through the nitride and oxide layers are done with a dry etch with one photoresist mask.

19. Regarding Claim 16, Tu et al. do not disclose that the first and second nitride layers are formed by LPCVD. Wu discloses that the first nitride layer (14) is formed by LPCVD (Col. 3,

lines 23 – 25) and that the second nitride layer (22) is formed by LPCVD (Col. 3, line 66 through Col. 4, line 3). It would have then been obvious to combine Wu with Tu et al. to obtain uniform nitride films.

16. Regarding Claim 17, Tu et al. disclose that functional devices within the integrated circuit are formed with LPCVD nitride layers. It would be obvious that PECVD could also be used to form the first and second layers of nitride, since both techniques produce a layer by CVD. In addition, commercial machines (Applied Materials,Novellus) are readily available in the art for plasma enhanced deposition. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form both nitride layers by PECVD to obtain high deposition rate films.

Response to Arguments

22. Arguments of Applicant with regard to Claims have been carefully considered, but these are considered moot in terms of the new ground(s) of rejection.

Conclusions

23. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703)**

872-9306.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
August 18, 2004